3.1 Consider the circuit shown in Figure P3.1.
(a) Show the truth table for the logic function f.
(b) If each gate in the circuit is implemented as a CMOS gate, how many transistors are needed?

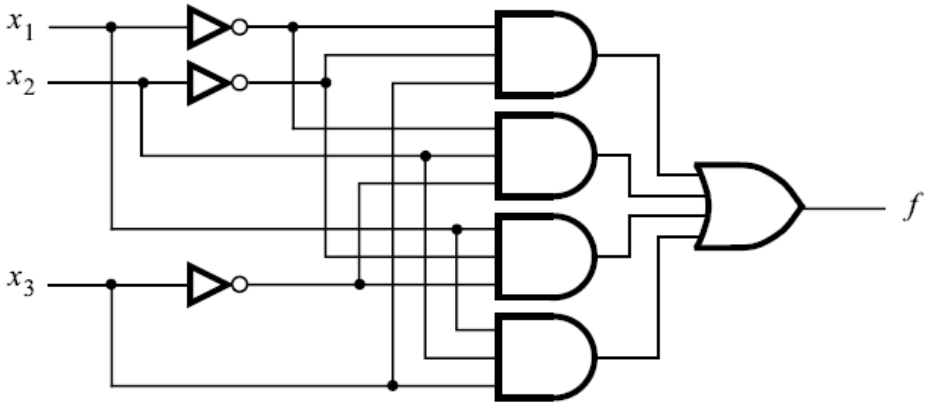

Figure 1 P3.1 A sum-of-products CMOS circuit.

Solution:

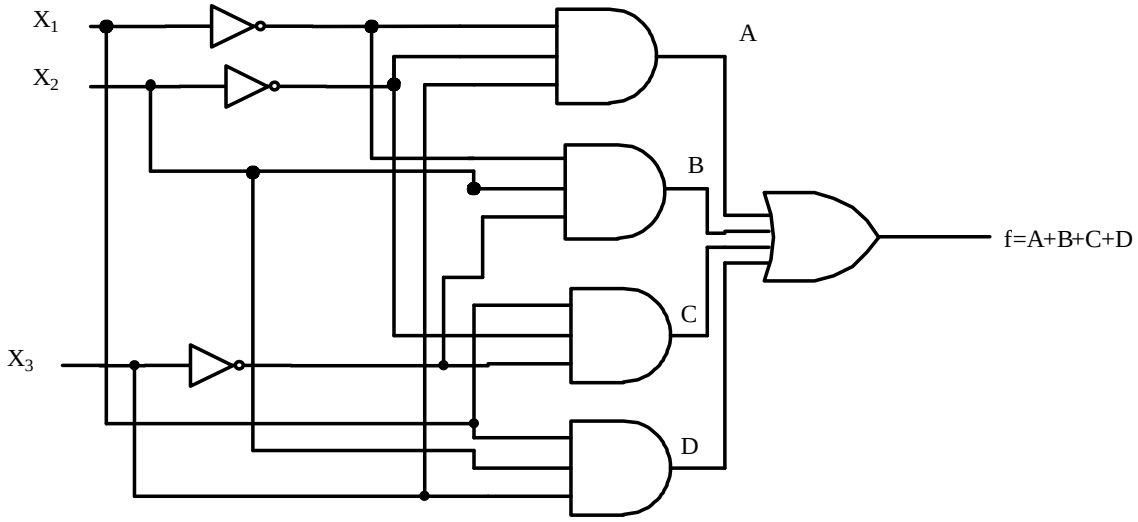

Figure 2

$$A = \overline{x_1}.\overline{x_2}.x_3$$
$$B = \overline{x_1}.x_2.\overline{x_3}$$
$$C = x_1.\overline{x_2}.\overline{x_3}$$
$$D = x_1.x_2.x_3$$
$$f = A + B + C + D$$

x_1	x_2	x_3	$A = \overline{x_1}.\overline{x_2}.x_3$	$B = \overline{x_1}.x_2.\overline{x_3}$	$C = x_1.\overline{x_2}.\overline{x_3}$	$D = x_1.x_2.x_3$	$f = A + B + C + D$
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**0**	**0**	**1**
0	**1**	**1**	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**	**1**	**0**	**1**
1	**0**	**1**	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**0**	**1**	**1**

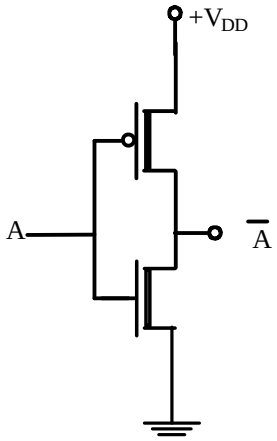

Figure 3 NOT gate requires 2 transistors

There are 3 three NOT gates. 3*2=6 transistors are required to build three NOT gates.

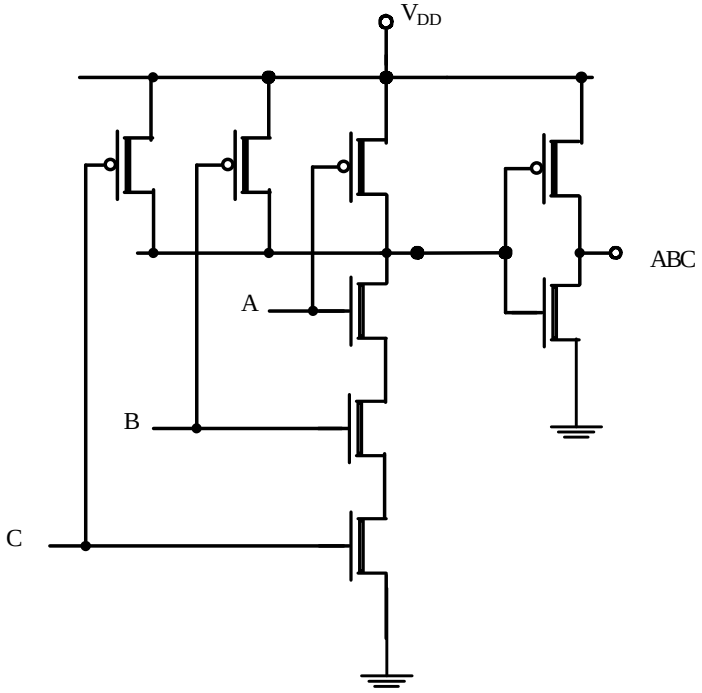

Figure 4 3-input AND gates requires 8 Transistors

Therefore 4 3-input AND gates require 4*8=32 transistors.

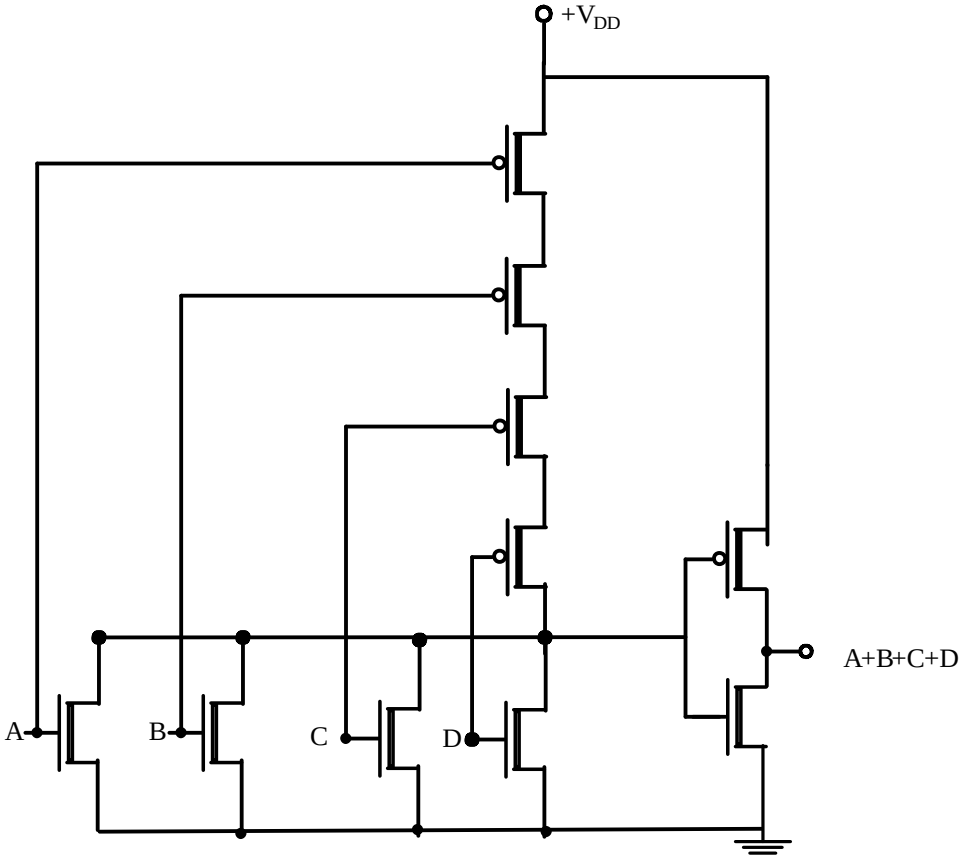

Figure 5 4-input OR gate requires 10 transistors

Number of transistors:

Gate	NOT	3-input AND	4-input OR
Number of Gates	3	4	1
Number of Transistors per Gate	2	8	10

So the total number of transistors = $2\times3+8\times4+10\times1=48$

3.2 (a) Show that the circuit in Figure P3.2 is functionally equivalent to the circuit in Figure P3.1.

(b) How many transistors are needed to build this CMOS circuit?

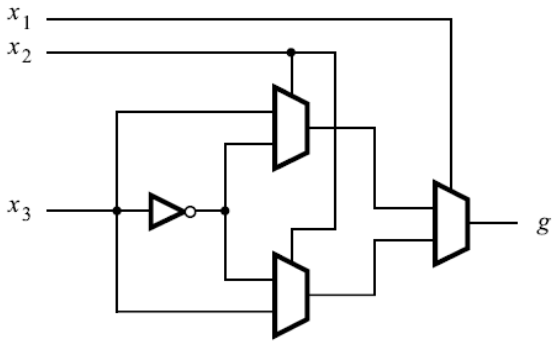

Figure 6

Solution:

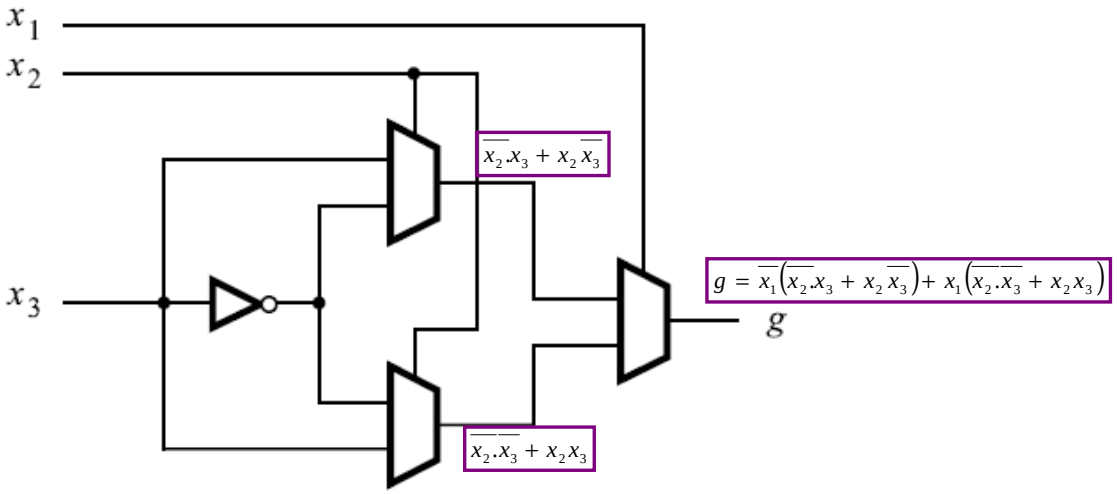

Figure 7

$$g = \overline{x_1}\left(\overline{x_2}.x_3 + x_2\overline{x_3}\right) + x_1\left(\overline{\overline{x_2}.x_3} + x_2x_3\right) = \overline{x_1}\,\overline{x_2}.x_3 + \overline{x_1}x_2\overline{x_3} + x_1\overline{x_2}.x_3 + x_1x_2x_3$$

This mathematical expression is similar to that obtained in Problem 3.1. Therefore these two circuit diagrams are functionally equivalent.

Assuming the multiplexers are implemented using transmission gates which is shown in figure 8.

Total number of transistors = NOT gates *2 + MUXes * 6

= (1*2) + (3*6) = 20

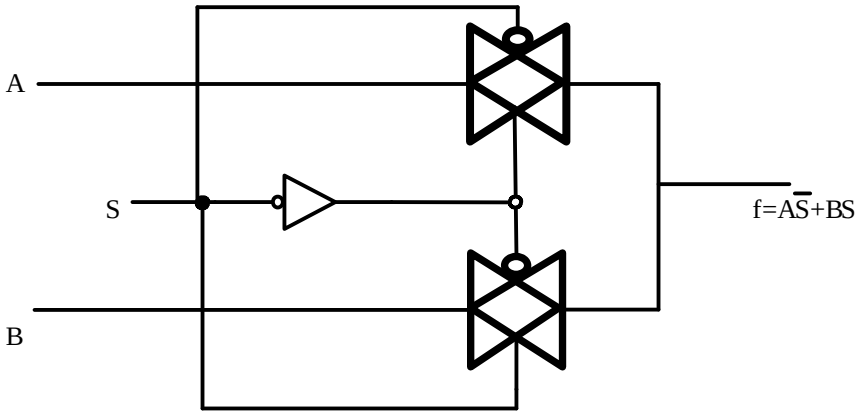

Figure 8 2-to-1 multiplexer built using transmission gates

Each transmission gate requires 6 transistors (4 for mux + 2 for inverter gate).

3.4. In Section 3.8.8 we said that a six-input CMOS AND gate can be constructed using two three-input AND gates and a two-input AND gate. This approach requires 22 transistors. Show how you can use only CMOS NAND and NOR gates to build the six-input AND gate, and calculate the number of transistors needed. (Hint: use DeMorgan's theorem.)

Solution:

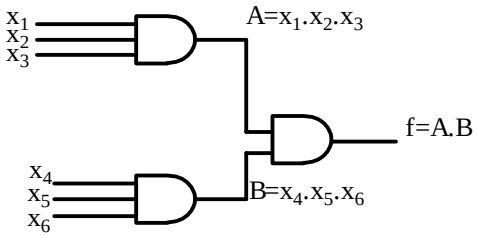

Figure 9

$$f = A.B$$

$$\bar{f} = \overline{A.B} = \overline{A} + \overline{B} = P + Q$$

$$f = \overline{\overline{A} + \overline{B}} = \overline{P + Q}$$

where, $P = \overline{A} = \overline{x_1.x_2.x_3}$ and $Q = \overline{B} = \overline{x_4.x_5.x_6}$

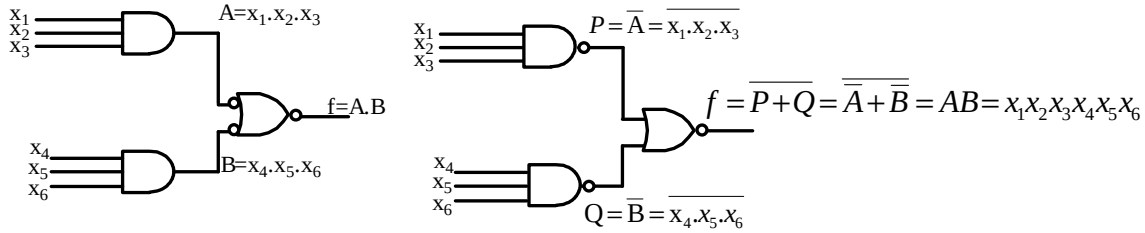

Figure 10

Total numbers of transistors =2*(3-input NAND gate)+1*(2-input NOR gate)=2*6+1*4=16

3.8 Figure P3.6 shows half of a CMOS circuit. Derive the other half that contains the PMOS transistors.

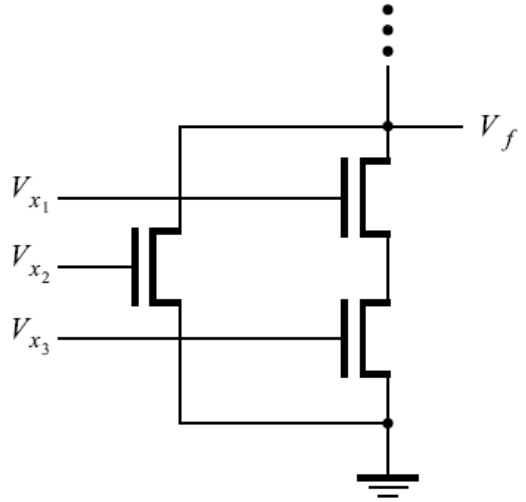

Figure 11 P3.6 The PDN in a CMOS circuit.

Solution:

The output of this digital circuit is,

$$v_f = v_{x_2} + v_{x_1}.v_{x_3}$$

The complement of the output is,

$$\overline{v_f} = \overline{v_{x_2} + v_{x_1}.v_{x_3}} = \overline{v_{x_2}}.\overline{v_{x_1}.v_{x_3}} = \overline{v_{x_2}}.\left(\overline{v_{x_1}} + \overline{v_{x_3}}\right)$$

Therefore the other half of the circuit will be,

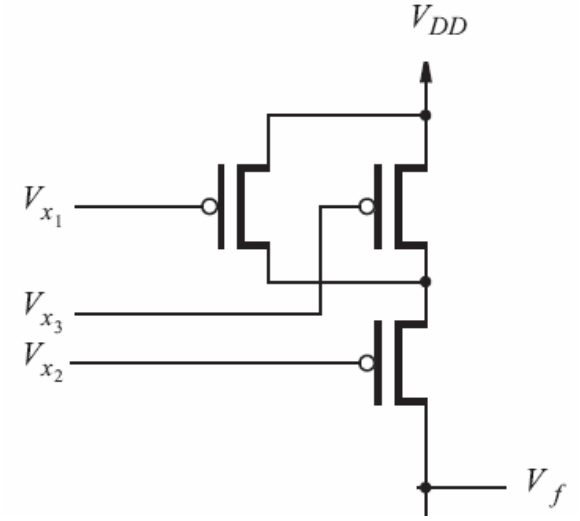

Figure 12 the other half of the circuit containing only PMOS transistors

The complete circuit is shown below

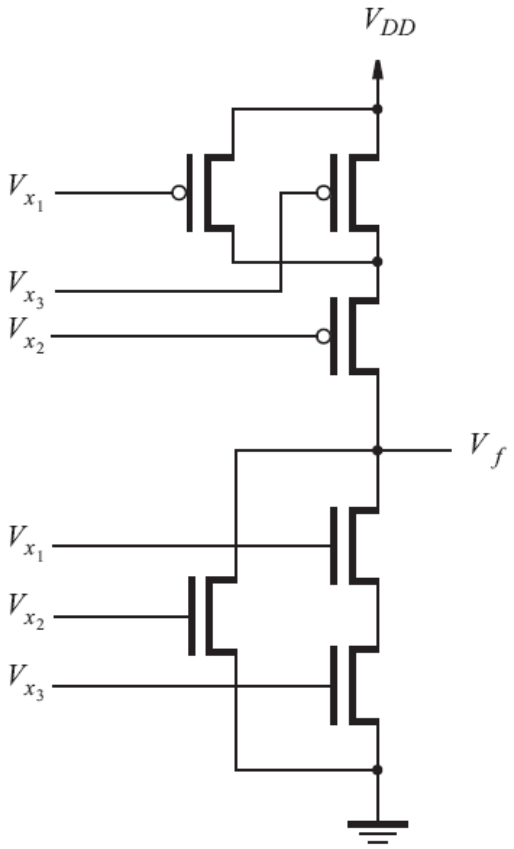

Figure 13 the complete circuit

3.9 Figure P3.7 shows half of a CMOS circuit. Derive the other half that contains the NMOS transistors.

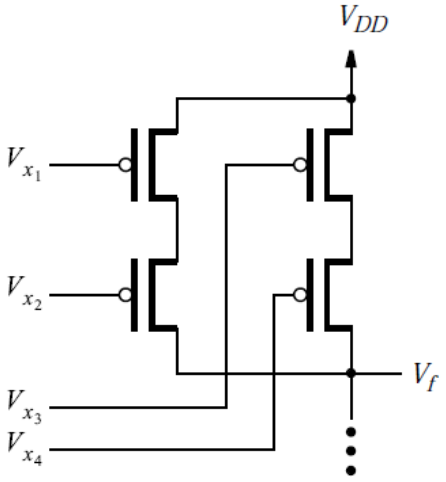

Figure 14 P3.7 The PUN in a CMOS circuit.

Solution: from the PUN of the circuit we get,

$$\overline{V_f} = \overline{V_{x1}}.\overline{V_{x2}} + \overline{V_{x3}}.\overline{V_{x4}}$$

$$V_f = \overline{\left(\overline{V_{x1}}.\overline{V_{x2}} + \overline{V_{x3}}.\overline{V_{x4}}\right)} = \left(\overline{\overline{V_{x1}}.\overline{V_{x2}}}\right).\left(\overline{\overline{V_{x3}}.\overline{V_{x4}}}\right) = \left(V_{x1} + V_{x2}\right)\left(V_{x3} + V_{x4}\right)$$

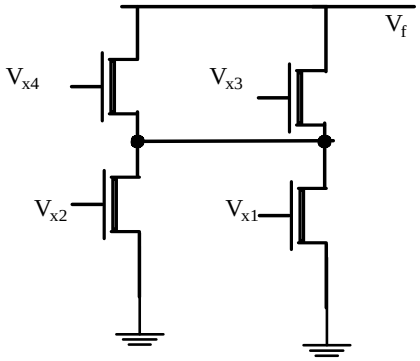

Figure 15 The PDN in a CMOS circuit

3.12 Derive a CMOS complex gate for the logic function f = xy +xz. Use as few transistors as possible (Hint: consider f).
Solution:
f=x(y+z)

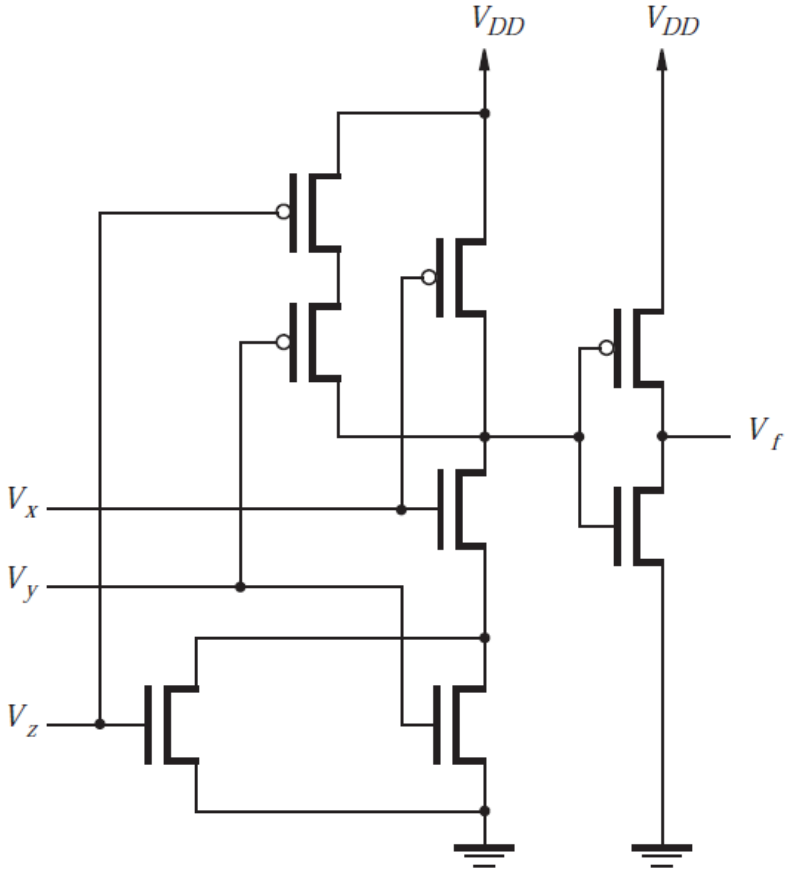

Figure 16

3.14 For an NMOS transistor, assume that k_n' = 20 μA/V^2, W/L = 2.5 μm/0.5 μm, VGS =5 V, and VT = 1 V. Calculate
(a) ID when VDS = 5 V
(b) ID when VDS = 0.2 V
Solution:
(a) Since V_{DS}>= V_{GS}-V_T, so the NMOS transistor is operating in the saturation region,

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_T)^2 = 10\frac{\mu A}{V^2}\times 5\times(5V-1V)^2 = 800\mu A$$

(b) In this case V_{DS}<V_{GS}-V_T, thus the NMOS transistor is operating in the triode region:

$$I_D = k_n'\frac{W}{L}\left\{(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right\} = 20\frac{\mu A}{V^2}\times 5\times\left[(5V-1V)\times 0.2V-\frac{1}{2}\times(0.2V)^2\right] = 78\mu A$$

3.17 For an NMOS transistor, assume that k_n' = 40 μA/V^2, W/L = 3.5 μm/0.35 μm, V_{GS} =3.3 V, and V_T = 0.66 V. For small V_{DS} , calculate R_{DS} .
Solution:
Here, W/L=10 and k_n'=0.040 mA/ V^2
Given, V_{DS} is small.
In this case V_{DS}<V_{GS}-V_T, thus the NMOS transistor is operating in the triode region:

$$I_D = k_n'\frac{W}{L}\left\{(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right\} \approx k_n'\frac{W}{L}(V_{GS}-V_T)V_{DS}$$

$$\Rightarrow R_{DS} = \frac{V_{DS}}{I_{DS}}$$

$$R_{DS} \cong \frac{V_{DS}}{k_n'\frac{W}{L}(V_{GS}-V_T)V_{DS}}$$

$$R_{DS} \cong \frac{1}{k_n'\frac{W}{L}(V_{GS}-V_T)} = \frac{1}{0.040\frac{mA}{V^2}\times 10\times(3.3V-.66V)} = 947\Omega$$