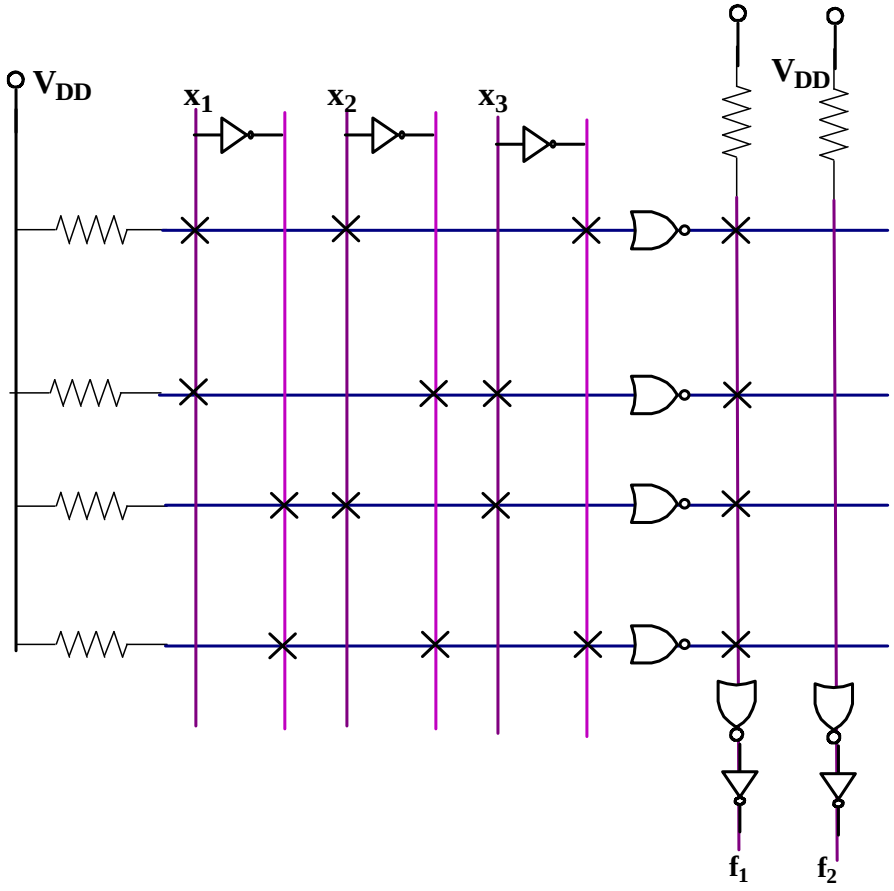
3.36 Using the style of drawing in Figure 3.66, draw a picture of a PLA programmed to implement $f_1(x_1, x_2, x_3) = \sum m(1, 2, 4, 7)$. The PLA should have the inputs $x_1, \ldots, x_3$; the product terms $P_1, \ldots, P_4$; and the outputs f_1 and f_2.

Solution:

$$f = \sum m(1,2,4,7) = \overline{x_1}.\overline{x_2}.x_3 + \overline{x_1}.x_2.\overline{x_3} + x_1.\overline{x_2}.\overline{x_3} + x_1.x_2.x_3$$



3.44 Consider the function $f(x_1, x_2, x_3) = x_1.\overline{x_2} + x_1x_3 + x_2.\overline{x_3}$. Show a circuit using 5 two-input lookup-tables (LUTs) to implement this expression. As shown in Figure 3.39, give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.

Solution:

$$f = x_1.\overline{x_2} + x_1x_3 + x_2.\overline{x_3}$$

x_1	x_2	$f_1 = x_1.\overline{x_2}$
0	0	0
0	1	0
1	0	1
1	1	0

x_1	x_3	$f_2 = x_1.x_3$
0	0	0
0	1	0
1	0	0
1	1	1

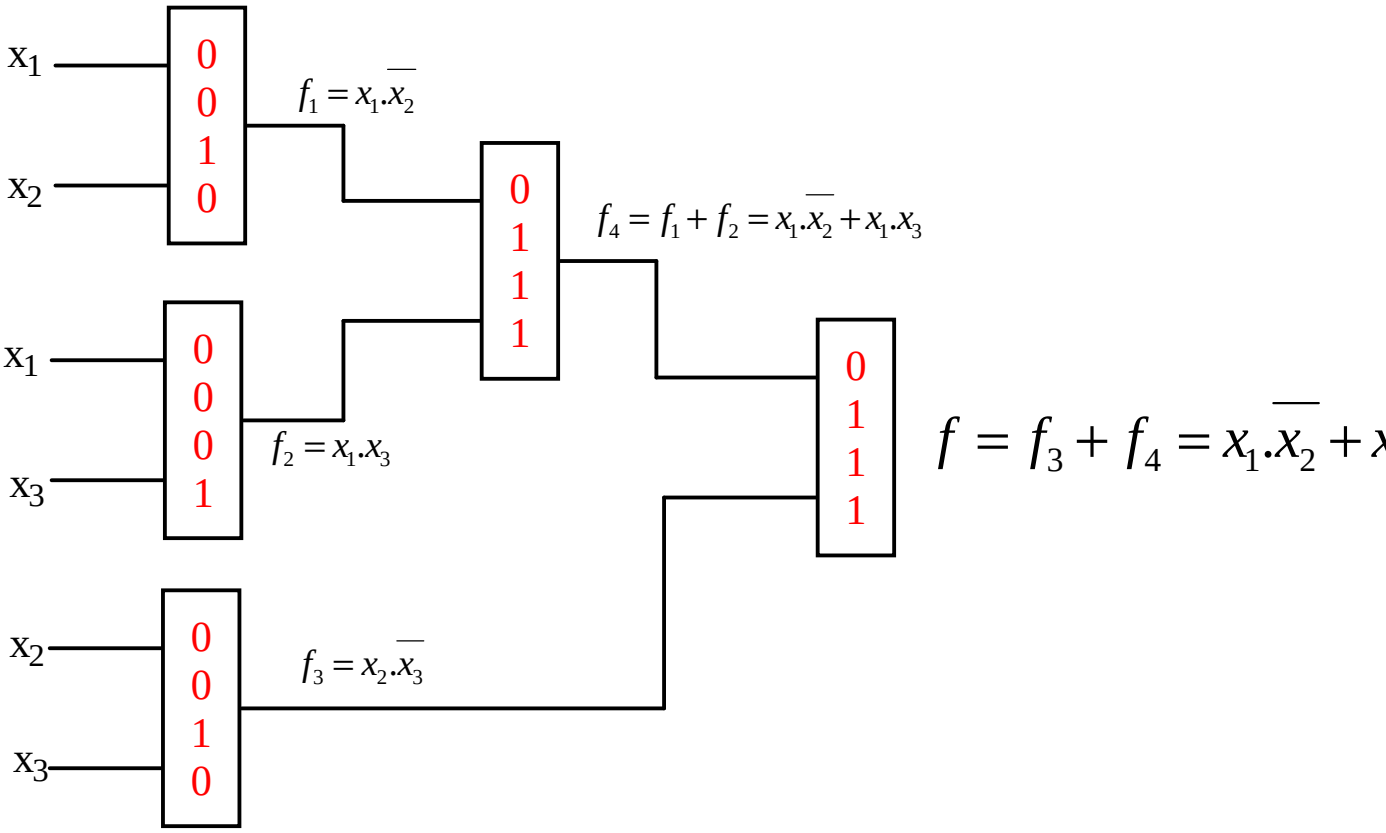
x_2	x_3	$f_3 = x_2.\overline{x_3}$
0	0	0
0	1	0
1	0	1
1	1	0

f_1	f_2	$f_4 = f_1 + f_2 = x_1\overline{x_2} + x_1.x_3$
0	0	0
0	1	1
1	0	1
1	1	1

f_4	f_3	$f = f_4 + f_3 = x_1\overline{x_2} + x_1.x_3 + x_2.\overline{x_3}$

0	0	0
0	1	1
1	0	1

1	1	1



3.45 Consider the function $f(x_1, x_2, x_3) = \sum m(2, 3, 4, 6, 7)$. Show how it can be realized using two two-input LUTs. As shown in Figure 3.39, give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.3.45

Solution:

$$f(x_1, x_2, x_3) = \sum m(2,3,4,6,7) = \overline{x_1}.x_2.\overline{x_3} + \overline{x_1}.x_2.x_3 + x_1.\overline{x_2}.\overline{x_3} + x_1.x_2.\overline{x_3} + x_1.x_2.x_3$$

$$f = \overline{x_1}.x_2.\overline{x_3} + \overline{x_1}.x_2.x_3 + x_1.\overline{x_2}.\overline{x_3} + x_1.x_2.\overline{x_3} + x_1.x_2.\overline{x_3} + x_1.x_2.x_3$$

$$f = \overline{x_1}.x_2(\overline{x_3} + x_3) + x_1.\overline{x_3}(\overline{x_2} + x_2) + x_1.x_2(\overline{x_3} + x_3)$$

$$f = \overline{x_1}.x_2.1 + x_1.\overline{x_3}.1 + x_1.x_2.1$$

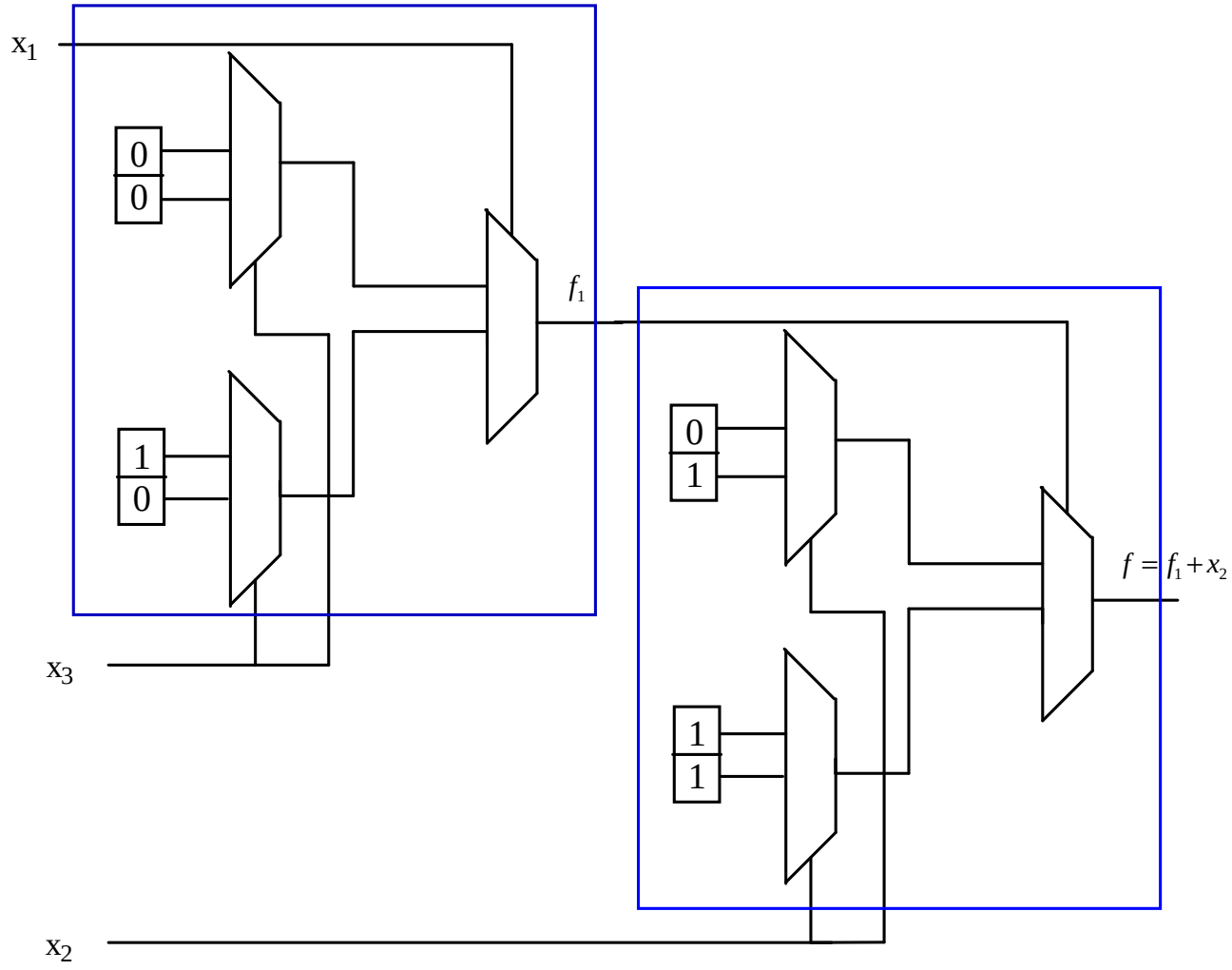
$$f = \overline{x_1}.x_2 + x_1.x_2 + x_1.\overline{x_3}$$

$$f = (\overline{x_1} + x_1).x_2 + x_1.\overline{x_3}$$

$$f = x_2 + x_1.\overline{x_3}$$

x_1	x_3	$f_1 = x_1.\overline{x_3}$
0	0	0
0	1	0
1	0	1
1	1	0

f_1	x_2	$f = f_1 + x_2 = x_1.\overline{x_3} + x_2$
0	0	0
0	1	1
1	0	1
1	1	1



3.49 Assume that a gate array contains the type of logic cell depicted in Figure P3.9. The inputs $in_1, \ldots, in_7$ can be connected to either 1 or 0, or to any logic signal.
(a) Show how the logic cell can be used to realize $f = x_1x_2 + x_3$.
(b) Show how the logic cell can be used to realize $f = x_1x_3 + x_2x_3$.

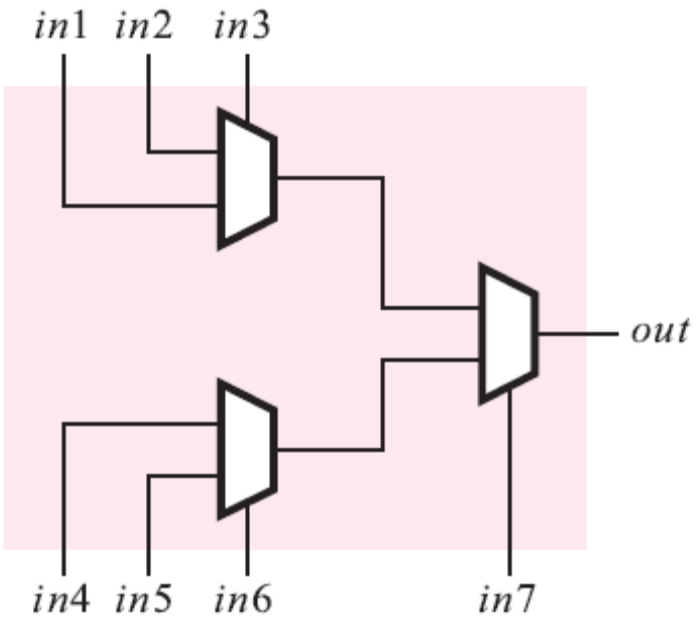


Figure P3.9 A gate-array logic cell.

Solution:
(a)

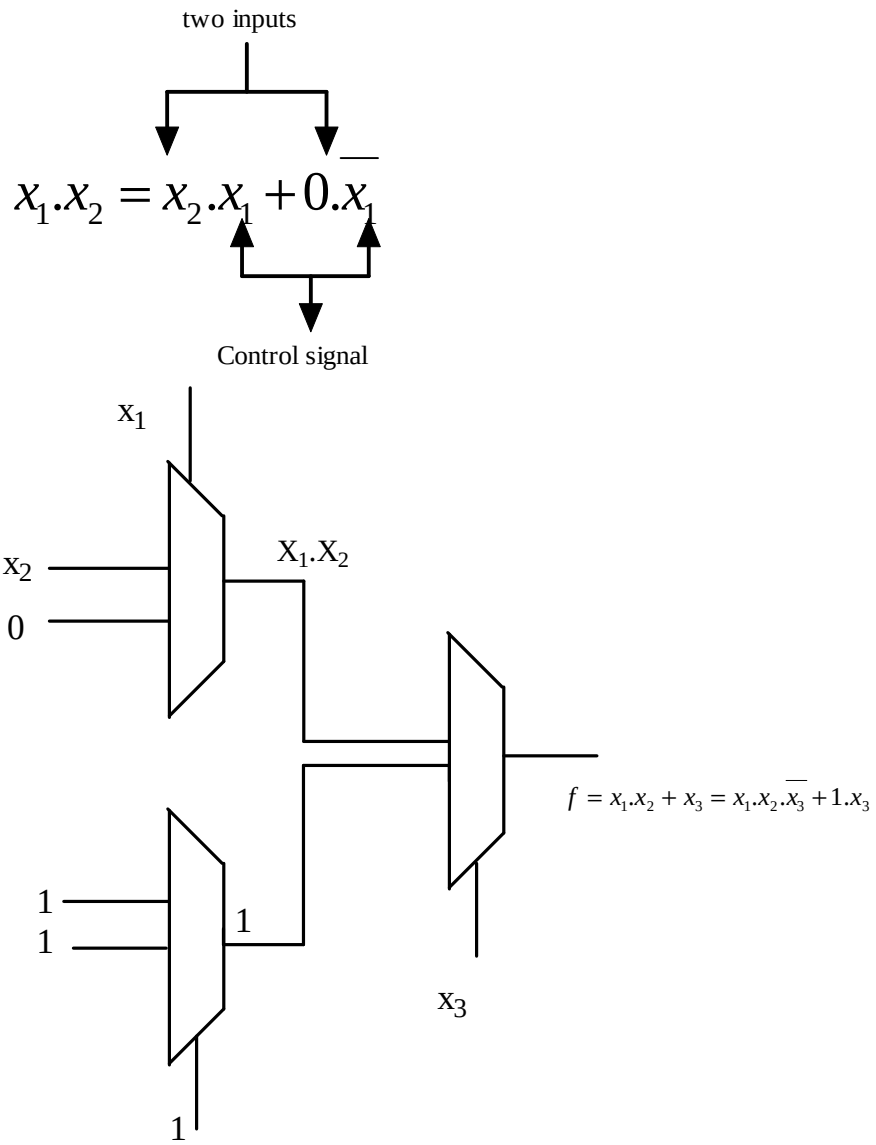
$$f = x_1.x_2 + x_3 = x_1.x_2.\overline{x_3} + 1.x_3$$

two inputs

$$f = x_1.x_2 + x_3 = x_1.x_2.\overline{x_3} + 1.x_3$$

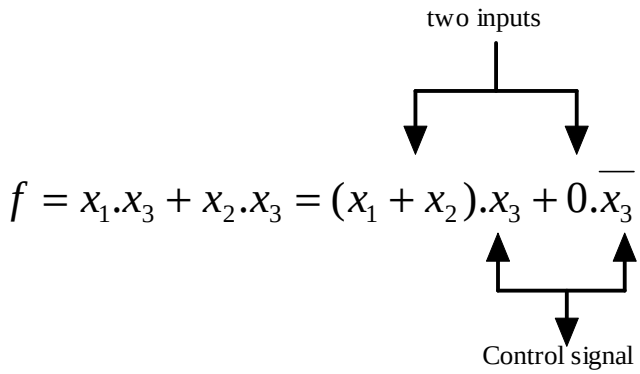
Control signal

Again

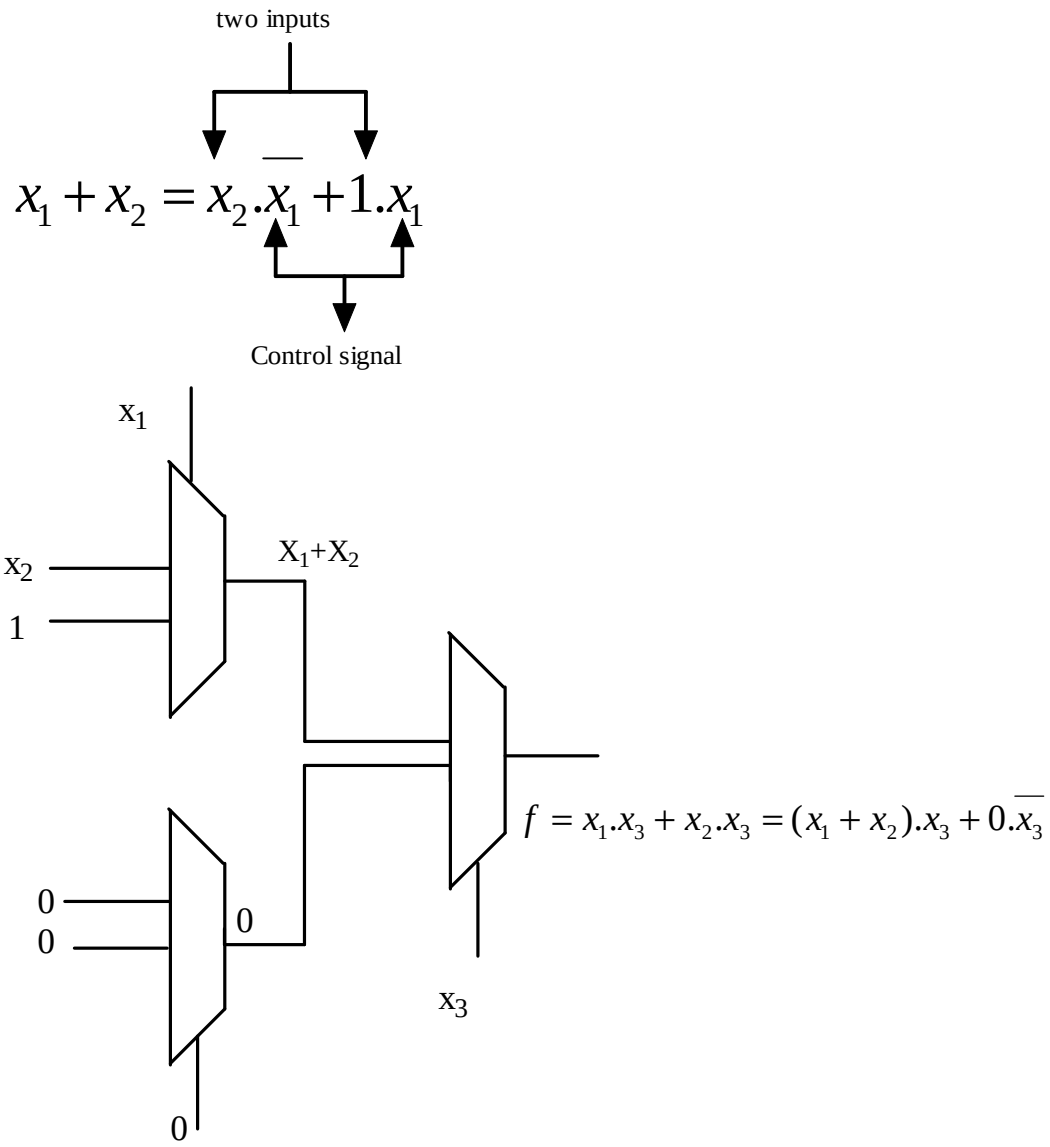


(b)

$f = x_1.x_3 + x_2.x_3 = (x_1 + x_2).x_3 + 0.\overline{x_3}$



Again



3.50 Assume that a gate array exists in which the logic cell used is a three-input NAND gate. The Inputs to each NAND gate can be connected to either 1 or 0, or to any logic signal. Show how the following logic functions can be realized in the gate array. (Hint: use DeMorgan's theorem.)

(a) $f = x_1.x_2 + x_3$ (b) $f = x_1 x_2 x_4 + x_2 x_3 \overline{x_4} + \overline{x_1}$

Solution:

(a)

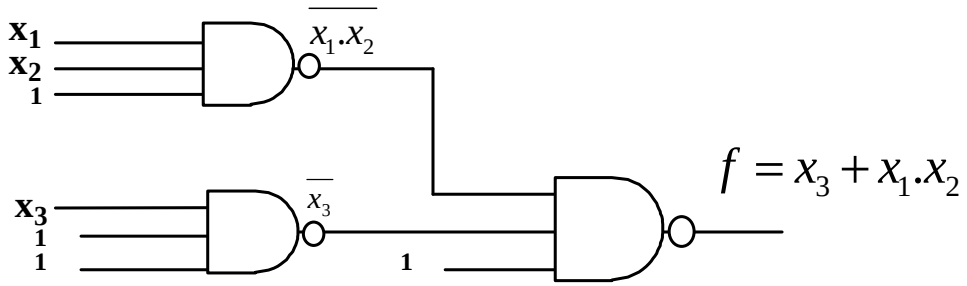
$f = x_1.x_2 + x_3$

$\bar{f} = \overline{x_1.x_2 + x_3} = \overline{x_1.x_2}..\overline{x_3} = P.Q$

$f = \overline{\overline{x_1.x_2}}..\overline{\overline{x_3}}$

Here P is output of a 3 input NAND gate with inouts: 1, x_1, x_2

And Q is output of a 3 input NAND gate with inouts: 1, 1, x_3

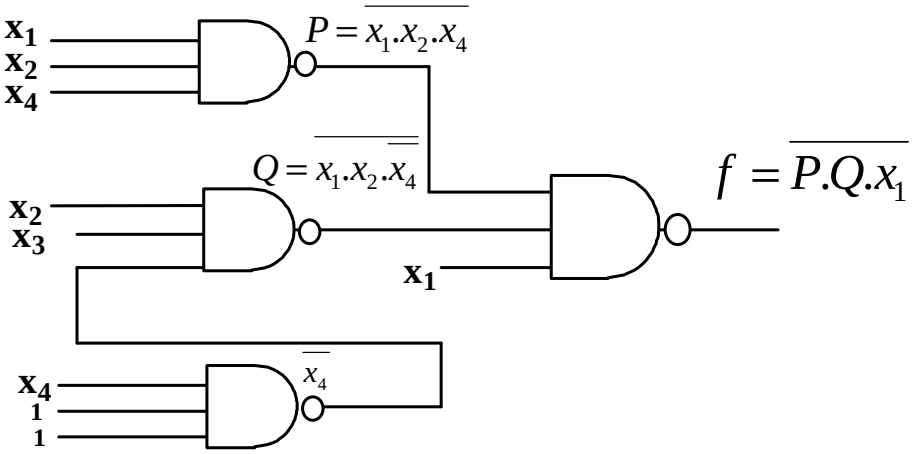


(b)

$f = x_1x_2x_4 + x_2x_3\overline{x_4} + \overline{x_1}$

$\bar{f} = \overline{x_1x_2x_4 + x_2x_3\overline{x_4} + \overline{x_1}} = \overline{x_1x_2x_4}.\overline{x_2x_3\overline{x_4}}.x_1 = P.Q.x_1$

$f = \overline{P.Q.x_1}$



3.54 What logic gate is realized by the circuit in Figure P3.10? Does this circuit suffer from any major drawbacks?

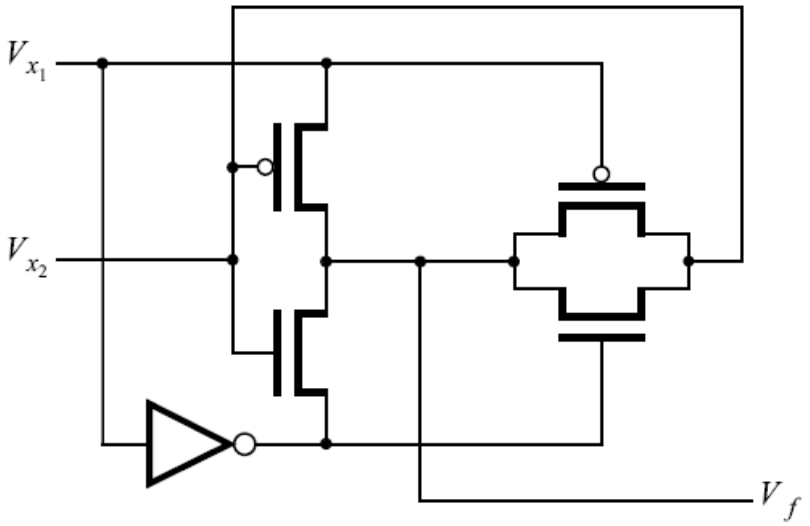


Figure P3.10 Circuit for problem 3.54.

Solution:
The circuit in Figure P3.10 is a two-input XOR gate. Since NMOS transistors are used only to pass logic 0 and PMOS transistors are used only to pass logic 1, the circuit does not suffer from any major drawbacks.

3.55 What logic gate is realized by the circuit in Figure P3.11? Does this circuit suffer from any major drawbacks?

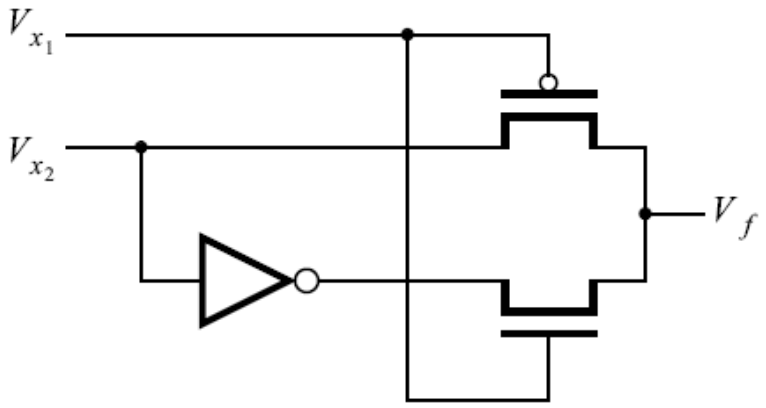


Figure P3.11 Circuit for problem 3.55.

Solution: The circuit in Figure P3.11 is a two-input XOR gate. The circuit has two major drawbacks.
1. when both the inputs are 0, the PMOS transistor must drive f to 0, resulting in f=Vt volts.
2. when V_{x1}=1and V_{x2}=0, the NMOS transistor must drive the output high, resulting f=V_{DD}-Vt