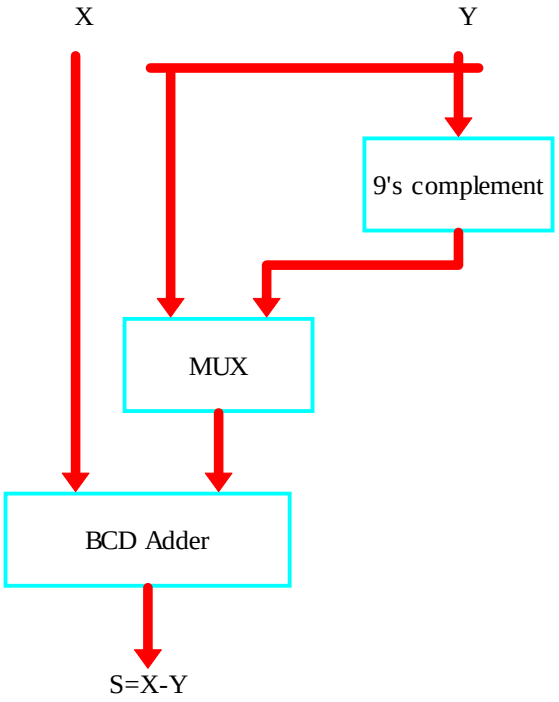
**5.17** Consider the VHDLcode in Figure P5.2. Given the relationship between the signals IN and OUT, what is the functionality of the circuit described by the code? Comment on whether or not this code represents a good style to use for the functionality that it represents.
Solution:
The code in Figure P5.2 represents a multiplier. It multiplies the lower two bits of Input by the upper two bits of Input, producing the four-bit Output.
The function of the circuit is not clear by observing the code. It's not a good style to write a code in terms of binary terms. It's better to write in a dataflow style.

**5.19** Derive a scheme for performing subtraction using BCD operands. Show a block diagram for the subtractor circuit.
Hint: Subtraction can be performed easily if the operands are in the 10'scomplement (radix complement) representation. In this representation the sign digit is 0 for a positive number and 9 for a negative number.
Solution:
Let, X and Y be BCD numbers




**5.25** Use algebraic manipulation to prove that $x \oplus (x \oplus y) = y$
Solution:

$$x \oplus (x \oplus y)$$
$$= x \oplus (x\bar{y} + \bar{x}y)$$
$$= x.\overline{(x\bar{y} + \bar{x}y)} + \bar{x}(x\bar{y} + \bar{x}y)$$
$$= x.(\bar{x}.\bar{y} + xy) + \bar{x}.x\bar{y} + \bar{x}y$$
$$= x..\bar{x}.\bar{y} + xy + 0 + \bar{x}y = 0 + y(x + \bar{x}) = y$$

**5.27** Figure 5.42 presents a general comparator circuit. Suppose we are interested only in determining whether 2 four-bit numbers are equal. Design the simplest circuit that can accomplish this task.
Solution:
Let, the inputs are A and B where both A and B are four digit numbers.

$A = a_3 a_2 a_1 a_0$

$B = b_3 b_2 b_1 b_0$

A and B will be equal if and only if ,

$a_3 = b_3$

$a_2 = b_2$

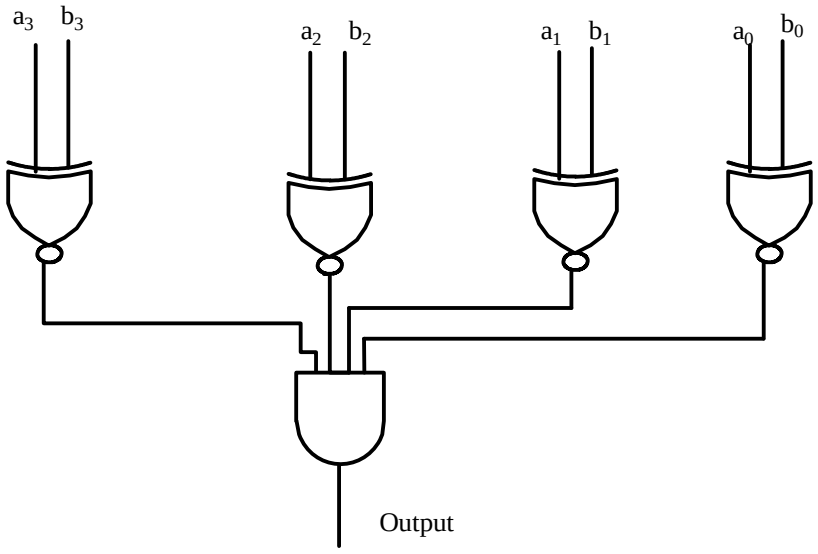
$a_1 = b_1$

$a_0 = b_0$

*Consider the truth table of XNOR gate which is the complement of XOR gate.*

| $a_0$ | $b_0$ | XNOR |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Circuit diagram:




**5.28** In a ternary number system there are three digits: 0, 1, and 2. Figure P5.3 defines a ternary half-adder. Design a circuit that implements this half-adder using binary-encoded signals, such that two bits are used for each ternary digit. Let *A* = $a_1a_0$, *B* = $b_1b_0$, and *Sum* = $s_1s_0$; note that *Carry* is just a binary signal. Use the following encoding: 00 = $(0)_3$, 01 = $(1)_3$, and 10 = $(2)_3$. Minimize the cost of the circuit.

Solution:

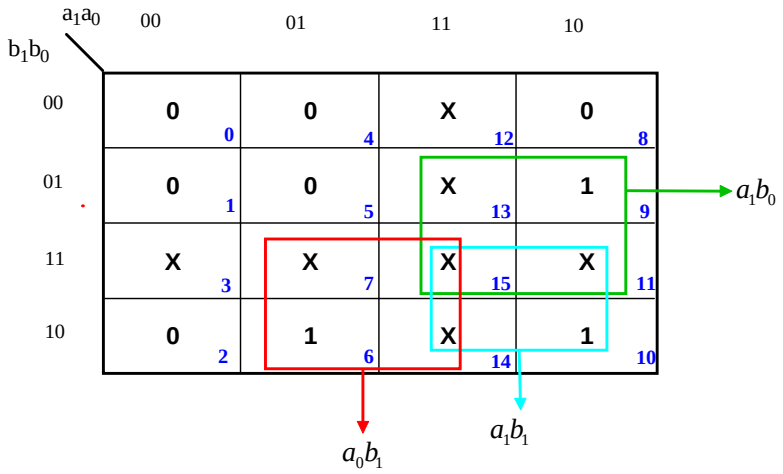
The truth table of the functions is:

| A | | B | | Carry | Sum | |
|---|---|---|---|---|---|---|
| $a_1$ | $a_0$ | $b_1$ | $b_0$ | | $s_1$ | $s_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | x | x | x |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | x | x | x |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | x | x | x |
| 1 | 1 | 0 | 0 | x | x | x |
| 1 | 1 | 0 | 1 | x | x | x |
| 1 | 1 | 1 | 0 | x | x | x |
| 1 | 1 | 1 | 1 | x | x | x |

To implement the function, Carry:

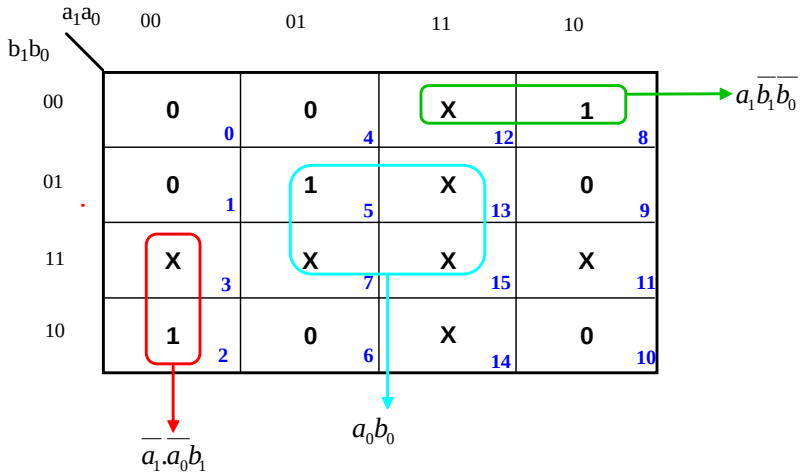
$$Carry(a_1,a_0,b_1,b_0)=\sum m(6,9,10)+D(3,7,11,12,1,14,15)$$




$$Carry(a_1,a_0,b_1,b_0)=a_0b_1+a_1b_1+a_1b_0$$

To implement the function $s_1$:

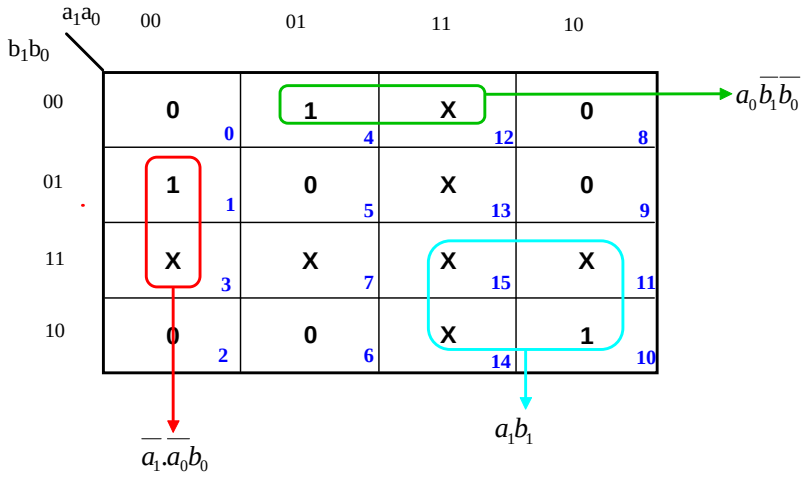
$$s_1(a_1,a_0,b_1,b_0)=\sum m(2,5,8)+D(3,7,11,12,1,14,15)$$




$$s_1(a_1,a_0,b_1,b_0)=\overline{a_1}\,\overline{a_0}b_1+a_0b_0+a_1\overline{b_1}\,\overline{b_0}$$

To implement the function $s_0$:

$$s_0(a_1,a_0,b_1,b_0) = \sum m(1,4,10) + D(3,7,11,12,1,14,15)$$




$$s_1(a_1,a_0,b_1,b_0) = \overline{a_1}\overline{a_0}b_0 + a_1b_1 + a_0\overline{b_1}\overline{b_0}$$

Circuit Diagram: